CLAIMS

I Claim:

1. A product term cell comprising:

a first floating gate structure located over a first p-channel transistor and a first n-channel transistor;

a second floating gate structure located over a second p-channel transistor and a second n-channel transistor;

a control gate structure capacitively coupled to the first and second floating gate structures;

a first tunnel oxide capacitor formed with the first floating gate structure;

a second tunnel oxide capacitor formed with the second floating gate structure;

a first transistor pair coupled between the first p-channel transistor and the second n-channel transistor; and

a second transistor pair coupled between the second p-channel transistor and the first n-channel transistor.

2. The product term cell of Claim 1, wherein source regions of the first p-channel transistor and the second p-channel transistor are coupled to a positive voltage supply terminal.

3. The product term cell of Claim 1, wherein source regions of the first n-channel transistor and the second n-channel transistor are coupled to a ground supply terminal.

4. The product term cell of Claim 1, wherein a source region of the first n-channel transistor is coupled to a first bit line, and a source region of the second n-channel transistor is coupled to a second bit line.

5. The product term cell of Claim 1, wherein the first transistor pair comprises:

a third p-channel transistor coupled between the first p-channel transistor and a first node; and

a third n-channel transistor coupled between the first node and the second n-channel transistor.

6. The product term cell of Claim 5, wherein the second transistor pair comprises:

a fourth p-channel transistor coupled between the second p-channel transistor and a second node; and

a fourth n-channel transistor coupled between the second node and the first n-channel transistor.

7. The product term cell of Claim 6, further comprising:

a first input terminal coupled to gates of the third p-channel transistor and the third n-channel transistor; and

a second input terminal coupled to gates of the fourth p-channel transistor and the fourth n-channel transistor.

8. The product term cell of Claim 7, further comprising an inverter coupled between the first and second input terminals.

9. The product term cell of Claim 6, further comprising an output terminal coupled to the first node and the second node.

10. The product term cell of Claim 9, further comprising a read transistor coupled to the output terminal.

11. The product term cell of Claim 10, wherein the read transistor comprises a fifth n-channel transistor having a source coupled to the ground supply voltage terminal, a drain coupled to the output terminal and a gate coupled to receive a read control signal.

12. A method of operating a product term cell having a first floating gate element and a second floating gate element, the method comprising:

erasing the first floating gate element, wherein erasing the first floating gate enables a first p-channel floating gate transistor that includes the first floating gate element and disables a first n-channel floating gate transistor that includes the first floating gate element; and

erasing the second floating gate element, wherein the erased second floating gate enables a second p-channel floating gate transistor that includes the second floating gate element and disables a second n-channel floating gate transistor that includes the second floating gate element.

13. The method of Claim 12, further comprising providing an output signal having a first logic state through the

enabled first p-channel floating gate transistor or the enabled second p-channel floating gate transistor.

14. The method of Claim 12, further comprising:

programming the first floating gate element, wherein the programmed first floating gate element disables the first p-channel floating gate transistor and enables the first n-channel floating gate transistor; and

applying a first input signal to a first transistor pair coupled between the second p-channel floating gate transistor and the first n-channel floating gate transistor.

15. The method of Claim 14, further comprising providing an output signal through the enabled first n-channel floating gate transistor or the enabled second p-channel floating gate transistor, in response to the first input signal.

16. The method of Claim 14, further comprising:

programming the second floating gate element, wherein the programmed second floating gate element disables the second p-channel floating gate transistor and enables the second n-channel floating gate transistor; and

applying a second input signal, complementary to the first input signal to a second transistor pair coupled between the first p-channel floating gate transistor and the second n-channel floating gate transistor.

17. The method of Claim 16, further comprising providing an output signal having a second logic state through the enabled first n-channel floating transistor or the second n-channel floating transistor.

18. The method of Claim 16, further comprising determining whether the first and second floating gate elements are programmed or erased.

19. The method of Claim 18, wherein the step of determining whether the first and second floating gate elements are programmed or erased comprises selecting the first and second input signals to have substantially equal voltage levels.

20. The method of claim 16, further comprising margin testing the programmed first and second floating gate elements.

21. The method of Claim 20, wherein the margin testing comprises:

applying a first read voltage to a control gate located over the first and second floating gate elements during a first read operation;

determining the presence of a read current above a threshold level during the first read operation;

applying a second read voltage, less than the first read voltage, to the control gate during a second read operation; and

determining the absence of a read current above the threshold level during the second read operation.

22. The method of Claim 14, wherein the step of programming the first floating gate element comprises:

applying a positive intermediate voltage to a control gate located over the first and second floating gate elements;

applying a positive programming voltage to a first tunnel oxide capacitor formed with the first floating gate element, the programming voltage being greater than the intermediate voltage; and then

lowering the voltage applied to the control gate to the ground supply voltage (0 Volts).

23. The method of Claim 12, wherein the steps of erasing the first and second floating gate elements further comprise applying a first erase voltage to a control gate located over the first and second floating gate elements.

24. The method of Claim 23, wherein the steps of erasing the first and second floating gate elements further comprise applying a second erase voltage to a first tunnel oxide capacitor coupled to the first floating gate element, and to a second tunnel oxide capacitor coupled to the second floating gate element.

25. A product term cell comprising:

means for storing a first charge that adjusts the threshold voltages of a first p-channel transistor and a first n-channel transistor;

means for storing a second charge that adjusts the threshold voltages of a second p-channel transistor and a second n-channel transistor;

means for selectively coupling either the first p-channel transistor or the second n-channel transistor to an output terminal; and

means for selectively coupling either the second p-channel transistor or the first n-channel transistor to the output terminal.